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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND

Technical Field

A method for manufacturing a semiconductor device is disclosed wherein a cylindrical capacitor is formed by selectively etching an oxide film in a cell area for preventing bridging between cells during a wet etching process of the oxide film in the cell area.

Figs. 1a to 1n are cross-sectional diagrams illustrating sequential steps of a conventional method for manufacturing a semiconductor device.

Referring to Fig. 1a, an interlayer insulating film 14 having a storage electrode contact 12 therein is formed on a semiconductor substrate 10 having a device isolation film (not shown), a word line (not shown) and a bit line (not shown) thereon. A nitride film 16, an oxide film 18, a hard mask 20 and a photoresist film (not shown) are sequentially formed on the interlayer insulating film 14, and the photoresist film is then patterned via a photolithography process to form a photoresist film pattern 22.

Referring to Fig. 1b, the hard mask 20, the oxide film 18 and the nitride film 16 are sequentially dry etched according to a conventional method using the photoresist film pattern 22 as a mask, to define a cell area C and a peripheral circuit area C.

Referring to Fig. 1c, the photoresist film pattern 22 and the hard mask 20 remaining after the dry etching process are removed.

Referring to Fig. 1d, a polysilicon layer (not shown) is deposited on the entire surface of the resulting structure, and then isolated via a chemical mechanical polishing (CMP) process to form a storage electrode 24.

Referring to Fig. 1e, the oxide film 18 in the cell area C and the peripheral circuit area P is removed by wet etching process so that only a storage electrode 24 remains.

Referring to Fig. 1f, a dielectric film 28 is formed by depositing a dielectric substance on the storage electrode 24.

Referring to Fig. 1g, a plate electrode 30 is formed by depositing a polysilicon layer on the dielectric film 28.

Referring to Fig. 1h, a photoresist film (not shown) is deposited on the entire surface of the resulting structure, and then selectively exposed and developed to form a plate mask 26 in a predetermined area of the plate electrode 30.

Referring to Fig. 1i, the plate electrode 30 is etched by using the plate mask 26, and then the plate mask 26 is removed.

Referring to Fig. 1j, an interlayer insulating film 36 is formed on the entire surface of the resulting structure. Large step difference is generated between the interlayer insulating film 36 formed in the cell area C and the interlayer insulating film 36 formed in the peripheral circuit area P. The step difference is required to be removed in a subsequent process.

Referring to Fig. 1k, a photoresist film (not shown) is deposited on the entire surface of the resulting structure. The photoresist film is then exposed and developed, to form a cell mask 34 on the interlayer insulating film 36 in the peripheral circuit area P.

Referring to Fig. 1l, the interlayer insulating film 36 in the cell area C is partially removed via a dry etching process using the cell mask 34.

Referring to Fig. 1m, the interlayer insulating film 36 under the cell mask 34 is partially removed by wet etching process.

Referring to Fig. 1n, the cell mask 34 is removed to form the interlayer insulating film 36 having its large step difference removed.

As described above, when the cylindrical capacitor is manufactured and the interlayer insulating film is formed on the resulting structure, a large step difference occurs between the interlayer insulating film formed in the cell area C and the interlayer insulating film formed in the peripheral circuit area P.

Additional processes are required to remove the large step difference, resulting in complication of the manufacturing process.

SUMMARY OF THE DISCLOSURE

A method for manufacturing a semiconductor device is disclosed wherein a cylindrical capacitor is formed by covering a peripheral circuit area with a photoresist film and selectively etching an oxide film in a cell area, and uses a new etching process for preventing bridging between cells from occurring when the oxide film is dried after the wet etching process is disclosed herein.

The method for manufacturing the semiconductor device comprises: (a) forming an oxide film for storage electrode on the entire surface of a semiconductor

substrate comprising a cell area and a peripheral circuit area; (b) etching the oxide film for storage electrode in the cell area to define a storage electrode area; (c) forming a storage electrode in the storage electrode area; (d) forming a photoresist film pattern on the oxide film for storage electrode in the peripheral circuit area; (e) removing the oxide film for a storage electrode in the cell area via a wet etching process using the photoresist film pattern as a mask, and removing the photoresist film pattern; (f) sequentially forming a dielectric film and a plate electrode on the entire surface of the resulting structure; and (g) forming an interlayer insulating film on the entire surface of the resulting structure.

The removing of the oxide film for a storage electrode in the cell area may employ a BOE (Buffered Oxide Etchant) solution bath using the photoresist film pattern as a mask, and the removing of the photoresist film pattern of the resulting structure may be performed in a Piranha solution bath, and may further comprise cleaning the resulting structure in an SC-1 solution bath and cleaning the resulting structure in a diluted HF solution bath.

In addition, the removing of the oxide film for a storage electrode in the cell area may employ a BHF (Buffered Hydrogen Fluoride) solution bath by using the photoresist film pattern as a mask, and cleaning the resulting structure in a pure water bath, and the removing of the photoresist film pattern of the resulting structure may be performed in a Piranha solution bath, and may further comprise cleaning the resulting structure in a pure water bath, and drying the resulting structure in a dryer.

According to another embodiment, a disclosed method may comprise: (a) removing an oxide film for a storage electrode in a cell area of a semiconductor substrate, wherein a storage electrode is disposed in the cell area, and a photoresist film pattern is disposed in peripheral circuit region of the semiconductor substrate by performing a wet etching process in a BHF (Buffered Hydrogen Fluoride) solution bath; (b) cleaning the resulting structure in a pure water bath; (c) removing the photoresist film pattern in a Piranha solution bath; (d) cleaning the resulting structure in a pure water bath; and (e) drying the resulting structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure will be described in terms of several embodiments to illustrate its broad teachings. Reference is also made to the attached drawings, wherein:

Figs. 1a to 1n are cross-sectional diagrams illustrating sequential steps of a conventional method for manufacturing a semiconductor device;

Figs. 2a to 2l are cross-sectional diagrams illustrating sequential steps of a method for manufacturing a semiconductor device in accordance with the present invention;

Figs. 3a and 3b are plane and sectional photographs showing results of the wet etching process of the oxide film in the cell area in Comparative Example 1, respectively;

Figs. 4a and 4b are plane and sectional photographs showing results of the wet etching process of the oxide film in the cell area in Comparative Example 2, respectively;

Figs. 5a and 5b are cross-sectional diagrams illustrating portion of a wet etching process of an oxide film in a cell area in Example 1;

Figs. 6a and 6b are plane and sectional photographs showing results of the wet etching process of the oxide film in the cell area in Example 1, respectively;

Figs. 7a and 7b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area in Examples 2, 3, 4 and 5; and

Figs. 8a and 8b are plane and sectional photographs showing results of the wet etching process of the oxide film in the cell area in Example 2, respectively.

DETAILED DESCRIPTION

The present disclosure will be described in detail with reference to the accompanying drawings.

Figs. 2a to 2l are cross-sectional diagrams illustrating sequential steps of a method for manufacturing a semiconductor device in accordance with the present invention.

Referring to Fig. 2a, an interlayer insulating film 114 having a storage electrode contact 112 therein is formed on a semiconductor substrate 110 having a device isolation film (not shown), a word line (not shown) and a bit line (not shown) thereon. A nitride film 116, an oxide film 118, a hard mask 120 and a photoresist film (not shown) are sequentially formed on the interlayer insulating film 114, and the photoresist film is then patterned via a photolithography process to form a photoresist film pattern 122.

Referring to Fig. 2b, the hard mask 120, the oxide film 118 and the nitride film 116 are sequentially dry etched according to a conventional method using the photoresist film pattern 122 as a mask, to define a cell area C and a peripheral circuit area C. Here, a guard ring 132 defined between the cell area C and the peripheral

circuit area P is covered by the photoresist film to prevent wet etching of the oxide film 118 in the peripheral circuit area P during a succeeding wet etching process of the oxide film 118 in the cell area C.

Referring to Fig. 2c, the photoresist film pattern 122 and the hard mask 120 remaining after the dry etching process are removed.

Referring to Fig. 2d, a polysilicon layer (not shown) is deposited on the entire surface of the resulting structure, and then isolated via a chemical mechanical polishing (CMP) process to form a storage electrode 124.

Referring to Fig. 2e, a photoresist film (not shown) is deposited on the entire surface of the resulting structure, and then selectively exposed and developed to form a "dip out" mask 126 which is a photoresist film pattern in the guard ring 132 and the peripheral circuit area P.

Referring to Fig. 2f, the oxide film 118 in the cell area C is removed by wet etching process.

Referring to Fig. 2g, the dip out mask 126 is removed by wet etching process so that only the storage electrode 124 remains.

The wet etching processes of Figs. 2f and 2g may be performed in a single wet station including a buffered oxide etchant (BOE) solution bath, a Piranha solution bath, an SC-1 solution bath and a diluted HF solution bath. In case of the wet etching process of the oxide film 118 in the cell area C shown in Fig. 2f, the wet etching process is preferably performed in the BOE solution bath, and in case of the wet etching process of the dip out mask 126 shown in Fig. 2g, the wet etching process is preferably performed in the Piranha solution bath, the SC-1 solution bath and the diluted HF solution bath.

In addition, the wet etching processes of Figs. 2f and 2g may be performed in a single wet station including a buffered hydrogen fluoride (BHF) solution bath, a pure water bath, a Piranha solution bath, a pure water bath and a dryer. In case of the wet etching process of the oxide film 118 in the cell area C shown in Fig. 2f, the wet etching process is preferably performed in the BHF solution bath and pure water bath, and in case of the wet etching process of the dip out mask 126 shown in Fig. 2g, the wet etching process is preferably performed in the Piranha solution bath, the pure water bath and the dryer.

The Piranha solution consists of H_2SO_4 and H_2O_2. Preferably, the volume ratio of H_2SO_4 to H_2O_2 is in the range of 2 : 1 to 6 : 1, and the temperature of the

Piranha solution ranges from 90 to 130°C, and more preferably, the volume ratio of H_2SO_4 to H_2O_2 is 4 : 1, and the temperature of the Piranha solution is about 120°C.

The oxidation of the surface of the storage electrode 124, namely conversion from hydrophobicity to hydrophilicity is possible, because the hydrophobic surface (Si-H) of the storage electrode 124 reacts with H_2O_2 in the Piranha solution and generates SiO_2 after the wet etching process of the oxide film 118 in the BOE solution or BHF solution, as represented by the following reaction formula:

$$Si + 2H_2O_2 \rightarrow SiO_2 + 2H_2O$$

The SC-1 solution consists of NH_4OH, H_2O_2 and H_2O. Preferably, the volume ratio of NH_4OH, H_2O_2 and H_2O is in the range of 1 : 1 : 20 to 1 : 5 : 50, and the temperature of the SC-1 solution ranges from 25 to 85°C, and more preferably the volume ratio of NH_4OH, H_2O_2 and H_2O is about 1 : 4 : 20, and the temperature of the SC-1 solution is 65°C.

In addition, the dryer is preferably an IPA steam dryer or Maragoni dryer. A spin dryer cannot be used since it generates bridging between cells due to the centrifugal force during a spin drying process.

Referring to Fig. 2h, a dielectric film 128 is formed by depositing a dielectric material on the storage electrode 124.

Referring to Fig. 2i, a plate electrode 130 is formed by depositing a polysilicon layer on the dielectric film 128.

Referring to Fig. 2j, a photoresist film (not shown) is deposited on the entire surface of the resulting structure, and selectively exposed and developed, to form a plate mask 134 in a predetermined area on the plate electrode 130.

Referring to Fig. 2k, the exposed plate electrode 130 is etched using the plate mask 134, and then the plate mask 134 is removed.

Referring to Fig. 2l, an interlayer insulating film 136 is formed on the entire surface of the resulting structure. Here, little step difference is generated between the interlayer insulating film 136 in the cell area C and the interlayer insulating film 136 in the peripheral circuit area P. Therefore, a subsequent process for removing the step difference is not needed.

The method for removing the oxide film in the cell area and the dip out mask will be explained by referring to Comparative Examples and Examples. However, the scope of the present invention is not limited to the Examples.

Comparative Example 1 : BOE solution bath→Dry etching process→Piranha solution bath→SC-1 solution bath→Diluted HF solution bath

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared.

An oxide film in the cell area was removed in a BOE solution bath, and then the dip out mask was removed via a dry etching process. Thereafter, photoresist residues of the resulting structure were removed in a Piranha solution (H_2SO_4 : H_2O_2 = 4 : 1 (volume ratio), at 120°C) bath, and oxide film and photoresist residues were then removed by sequentially performing cleaning processes in an SC-1 solution bath and a diluted HF solution bath. As shown in Figs. 3a and 3b, bridging (indicated by A) was generated between cells.

Comparative Example 2 : BHF solution bath→Pure water bath→Dryer→Dry etching process of dip out mask

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared.

An oxide film in the cell area was removed in a BHF solution (contains over 0.5% of HF) bath, and then the resulting structure was cleaned in a pure water bath and dried using an IPA steam dryer.

The dip out mask was then removed via a dry etching process. As shown in Figs. 4a and 4b, bridging which is indicated as A, was generated between cells.

In the wet etching process of Comparative Example 2, since the polysilicon storage electrode is exposed, the surface of the storage electrode is subjected to the drying process in an Si-H hydrophobic state. The dip out mask dissolves in isopropyl alcohol since the IPA steam dryer is used. The dip out mask dissolved in isopropyl alcohol serves as a carbon source on the hydrophobic surface of the storage electrode, which causes drying failure due to water spots. Such drying failure results in bridging between cells.

Example 1 : BOE solution bath→Piranha solution bath→SC-1 solution bath→Dilluted HF solution bath

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared. A wet etching process of the semiconductor device was performed in a single wet station including a BOE solution bath, a Piranha solution bath, an SC-1 solution bath and a diluted HF solution bath.

Figs. 5a and 5b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area.

Referring to Fig. 5a, the oxide film 118 in the cell area C is removed in the BOE solution bath 100 while the peripheral circuit area P is covered by the dip out mask 126.

Referring to 5b, the dip out mask 126 is removed in the Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$ (volume ratio), at 120°C) bath 104, and the surface of the storage electrode 124 is oxidized, i.e. converted from hydrophobic to hydrophilic.

Thereafter, photoresist residues of the resulting structure were removed in the SC-1 solution ($NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$ (volume ratio), at 65°C) bath, and oxide film and photoresist residues were then removed in the diluted HF solution bath. As shown in Figs. 6a and 6b, bridging between cells did not occur in the resulting semiconductor device.

Example 2 : BHF solution bath→Pure water bath→Piranha solution bath→Pure water bath→Dryer

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared. A wet etching process of the semiconductor device was performed in a single wet station including a BHF solution bath, a pure water bath, a Piranha solution bath, a pure water bath and a dryer.

Figs. 7a and 7b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area.

Referring to Fig. 7a, the oxide film 118 in the cell area C is removed in the BHF solution bath 102 (contains over 0.5% of HF) while the peripheral circuit area P is covered by the dip out mask 126.

The resulting structure is cleaned in the pure water bath.

Referring to Fig. 7b, the dip out mask 126 is removed in the Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$ (volume ratio), at 120°C) bath 104, and the surface of the storage electrode 124 is oxidized, i.e. converted from hydrophobic to hydrophilic.

Thereafter, the resulting structure was cleaned in the pure water bath, and dried using an IPA stream dryer. As shown in Figs. 8a and 8b, bridging between cells did not occur in the resulting semiconductor device.

<u>Example 3 : BHF solution bath→Pure water bath→Piranha solution bath→Pure water bath→SC-1 solution bath→Pure water bath→Dryer</u>

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared. A wet etching process of the semiconductor device was performed in a single wet station including a BHF solution bath, a pure water bath, a Piranha solution bath, a pure water bath, an SC-1 solution bath, a pure water bath and a dryer.

Figs. 7a and 7b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area explained in the second example.

Referring to Fig. 7a, the oxide film 118 in the cell area C is removed in the BHF solution bath 102 (contains over 0.5% of HF) while the peripheral circuit area P is covered by the dip out mask 126.

The resulting structure is cleaned in the pure water bath.

Referring to Fig. 7b, the dip out mask 126 is removed in the Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$ (volume ratio), at 120°C) bath 104, and the surface of the storage electrode 124 is oxidized, i.e. converted from hydrophobic to hydrophilic.

Thereafter, the resulting structure was cleaned in the pure water bath, photoresist residues were removed in the SC-1 solution ($NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$ (volume ratio), at 65°C) bath, and the resulting structure was re-cleaned in the pure water bath and dried using an IPA stream dryer. As a result, bridging between cells did not occur in the resulting semiconductor device.

<u>Example 4 : BHF solution bath→Pure water bath→Piranha solution bath→Pure water bath→SC-1 solution bath→Pure water bath→dilluted HF solution bath→Pure water bath→Dryer</u>

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared. A wet etching process of the semiconductor device was performed in a single wet station including a BHF solution bath, a pure water bath, a Piranha solution

bath, a pure water bath, an SC-1 solution bath, a pure water bath, a diluted HF solution bath, a pure water bath and a dryer.

Figs. 7a and 7b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area explained in the second example.

Referring to Fig. 7a, the oxide film 118 in the cell area C is removed in the BHF solution bath 102 (contains over 0.5% of HF) while the peripheral circuit area P is covered by the dip out mask 126.

The resulting structure is cleaned in the pure water bath.

Referring to Fig. 7b, the dip out mask 126 is removed in the Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$ (volume ratio), at 120°C) bath 104, and the surface of the storage electrode 124 is oxidized, i.e. converted from hydrophobic to hydrophilic.

Thereafter, the resulting structure was cleaned in the pure water bath, photoresist residues were removed in the SC-1 solution ($NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$ (volume ratio), at 65°C) bath, the resulting structure was re-cleaned in the pure water bath, and photoresist and oxide film residues on the storage electrode were removed in the diluted HF solution bath.

Next, the resulting structure was cleaned in the pure water bath and dried using an IPA stream dryer. A subsequent deposition process of a dielectric film was performed via a conventional method. As a result, bridging between cells did not occur in the resulting semiconductor device.

<u>Example 5 : BHF solution bath→Pure water bath→Piranha solution bath→Pure water bath→dilluted HF solution bath→Pure water bath→SC-1 solution bath→Pure water bath→Dryer</u>

A semiconductor device including a cell area having a storage electrode formed therein and a peripheral circuit area having a dip out mask formed therein was prepared. A wet etching process of the semiconductor device was performed in a single wet station including a BHF solution bath, a pure water bath, a Piranha solution bath, a pure water bath, a diluted HF solution bath, a pure water bath, an SC-1 solution bath, a pure water bath and a dryer.

Figs. 7a and 7b are cross-sectional diagrams illustrating portion of the wet etching process of the oxide film in the cell area explained in the second example.

Referring to Fig. 7a, the oxide film 118 in the cell area C is removed in the BHF solution bath 102 (contains over 0.5% of HF) while the peripheral circuit area P is covered by the dip out mask 126.

The resulting structure is cleaned in the pure water bath.

Referring to Fig. 7b, the dip out mask 126 is removed in the Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$ (volume ratio), at 120°C) bath 104, and the surface of the storage electrode 124 is oxidized, i.e. converted from hydrophobic to hydrophilic.

Thereafter, the resulting structure was cleaned in the pure water bath, photoresist residues and an oxide film on the surface of a storage electrode were removed in the diluted HF solution bath, the resulting structure was re-cleaned in the pure water bath, and particles were removed in the SC-1 solution ($NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$ (volume ratio), at 65°C) bath.

Next, the resulting structure was cleaned in the pure water bath and dried using an IPA stream dryer. A subsequent deposition process of a dielectric film was performed via a conventional method. As a result, bridging between cells did not occur in the resulting semiconductor device.

As discussed above, step difference between the interlayer insulating film formed in the cell area and the interlayer insulating film formed in the peripheral circuit area is minimized by covering the peripheral circuit area by the photoresist film and selectively etching the oxide film in the cell area to form a cylindrical capacitor, thereby simplifying the manufacturing process.

In addition, bridging between the cells is prevented by performing a simple wet etching process using a single wet station, without performing a separate dry etching process for removing the oxide film and the photoresist film pattern, thereby improving the yield of the device.